IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LINEAR TECHNOLOGY CORPORATION, Plaintiff, v. MONOLITHIC POWER SYSTEMS, INC., Defendant.	)	C.A. No. 06-476-GMS **JURY TRIAL DEMANDED** **PUBLIC VERSION**

MONOLITHIC POWER SYSTEMS' OPPOSITION TO LINEAR'S MOTION IN LIMINE NO. 1 TO PRECLUDE MPS FROM OFFERING AT TRIAL EVIDENCE AND/OR ARGUMENT THAT THE ASSERTED CLAIMS ARE LIMITED TO TWO STATES OF OPERATION

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I. INTRODUCTION

Through its motion *in limine* number 1, Linear asks the Court to reopen claim construction and, in essence, to grant partial summary judgment as to one of MPS's non-infringement arguments. This is improper. The Court has issued its claim constructions. MPS's non-infringement positions and Dr. Szepesi's Answering Expert Report are consistent with those constructions. Thus, Linear's motion is without merit.

MPS's argument that the MP1543 cannot and does not infringe the asserted claims because it does not have the two states of circuit operation set forth in the patent claims is based on the plain language of the claims. This plain meaning is confirmed by the specification and by the prosecution history. Linear had its chance to identify and argue claim construction issues; the Court set a schedule for doing so. Now, however, it appears that Linear realizes that a plain reading of the claims does not support its infringement theory and so it seeks another bite at the apple. The Court should reject Linear's attempt to end-run the Court's schedule. Furthermore, were the Court to entertain Linear's invitation to re-construe the claims, it should reject Linear's incorrect position in light of the intrinsic evidence.

II. THE ACCUSED MP1543 PRODUCT CANNOT AND DOES NOT INFRINGE UNDER THE COURT'S CLAIM CONSTRUCTIONS

The asserted claims describe a voltage regulator that transitions between two states of operation, described as the "first state of circuit operation" and the "second state of circuit operation." From the outset, MPS has contended that a voltage regulator built using the accused MP1543 product does not have the claimed "second state of circuit operation." In fact, such a voltage regulator does not transition from a continuous conduction state (which Linear contends is the "first state of circuit operation") to a pulse skipping state (which Linear contends is the "second state of circuit operation") when the current supplied to the load falls below a threshold

fraction of the maximum rated output current. Instead, as explained in Dr. Szepesi's Answering Report, if such a voltage regulator transitions from a "continuous conduction" state, it transitions into a "discontinuous conduction" state, which Linear does not contend is the "second state of circuit operation." Such a regulator may then remain in the discontinuous conduction state or it may transition back to the continuous conduction state or to the "pulse skipping" state that Linear contends is the claimed "second state." *See* Answering Expert Report of Dr. Szepesi at 27-42 (Ex. 1). Either way, the MP1543 does not infringe. *See id.*, at 71.

III. MPS NEVER WAIVED A CLAIM CONSTRUCTION ARGUMENT

Linear argues that MPS is bound to follow the Court's Claim Construction Order. MPS agrees. So is Linear. Here, it is Linear that seeks to deviate from the Court's order. If anyone has waived its argument, it is Linear. In its Motion, Linear never argues that Dr. Szepesi's stated opinion is inconsistent with the Court's claim construction – just that it is not addressed by it. Thus, Linear's citation to *Tivo, Inc. v. Echostar Communications Corp.,* 516 F.3d 1290 (Fed. Cir. 2008), is a red herring. In *Tivo,* the district court properly prevented an expert from testifying in the alternative first under the court's claim construction and second under the construction put forth by the opposing party's expert. *Id.* at 1311. This is not what Linear is accusing MPS of doing and thus *Tivo* has no relevance to the instant motion.

Because Linear is raising a new argument, it is not surprising that the Court did not resolve this dispute in the Claim Construction Order. *See Vanderlande Indus. Nederland BV v. U.S. Int'l Trade Comm'n,* 366 F.3d 1311, 1323 (Fed. Cir. 2004) ("First, this claim limitation was not in dispute when the ALJ construed the claims, and thus there was no reason for the ALJ to set out a formal construction."). In this case, the plain meaning of the claims is clear, and there is no reason to re-construe the claims or artificially limit Dr. Szepesi's testimony to account for Linear's new dispute. *See Unitherm Food Sys., Inc. v. Swift-Eckrich, Inc.,* 375 F.3d 1341, 1350

(Fed. Cir. 2004) ("Presumably, all other claim terms were undisputed because one of ordinary skill in the art would understand their plain meanings.").

In any event, were the Court to conclude that further clarification was necessary as to the meaning of claim terms, it would have the discretion to provide that clarification. The Federal Circuit has rejected Linear's implication that the Court must resolve all claim construction disputes in a formal *Markman* hearing. *See, e.g., Ballard Med. Prods. v. Allegiance Healthcare Corp.*, 268 F.3d 1352, 1358 (Fed. Cir. 2001).

IV. THE COURT SHOULD REJECT LINEAR'S BROADENING "CONSTRUCTION"

The plain meaning of the claims excludes a third state of circuit operation between the first and second states of circuit operation. Claim 41 of the '178 patent (emphasis added), for example, claims:

> turning both switching transistors simultaneously OFF for a period of time during a second state of circuit operation ***following*** the first state of circuit operation, . . . ***the period of time beginning*** when the current supplied to the load falls below a threshold fraction of maximum rated output current for the regulator, and having a duration which is a function of the current supplied to the load by the regulator;

The claim language thus makes clear that (1) the second state of circuit operations "follow[s]" the first state of circuit operation (not some unidentified third state of circuit operation) and (2) the transition from the first state of circuit operation to the second state of circuit operation occurs "when the current supplied to the load falls below a threshold fraction of maximum rated output current . . . ." "Because the patentee is required to 'define precisely what his invention is,' the [Supreme] Court explained, it is 'unjust to the public, as well as an evasion of the law, to construe it in a manner different from the plain import of its terms.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *White v. Dunbar*, 119 U.S. 47 (1886)).

The ordinary meaning of the claims is further supported by the specification, which describes the invention similarly:

> At high load current levels (e.g., greater than 20 percent of the maximum rated output current) control circuit 70 operates similar to control circuit 35 of [prior art] FIG. 1. . . . In accordance with the present invention, regulator circuit 50 goes into sleep mode at low output current levels . . . .

'178 patent, at 6:17-35. *See also id.*, at 12:14-59. As the specification explains, when the load current crosses the threshold fraction of maximum rated output current, the invention transitions from the first state of circuit operation to the second state of circuit operation, without any intervening states of operation.

Finally, the prosecution history confirms the plain meaning of the claims. In an effort to overcome a prior art rejection by the patent examiner, Linear explicitly defined its invention as a "two-state" invention:

> Applicants' ***invention*** is directed to maintaining high efficiency in a switching voltage regulator circuit by ***providing two states of circuit operation***. . . . When the output current of the regulator drops below a threshold level--i.e. below some fraction (e-g., 20%) of the regulator's maximum rated output current--the regulator's switching transistors are turned off simultaneously for a period of time while previously stored energy in the regulator's output circuit supplies current to the load. This ***two-state technique for improving efficiency*** would not have been obvious from an AC power source circuit that disables its output during an overload (the asserted combination of Inam and Josephson), or from an AC power source that goes into a sleep mode when it is not functioning (Inam and Fung).

June 5, 1995 Response to Examiner's Action, at 6 (Ex. 2).

Likewise, in amending their claims to "more particularly point out and distinctly claim" their invention, the inventors explained that "the threshold output current ***dividing the two states of operation*** of the regulator is a fraction of the regulator's maximum rated output current . . . ." *Id.* at 8 (emphasis added). Only then did the Examiner allow the claims to issue. (Ex. 3).

Thus, to the extent that there is any ambiguity in the language of the claims (which MPS believes there is not), Linear surrendered and disclaimed any coverage of a supposed third state

of circuit operation between the first and second states of circuit operation. *See Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1374 (Fed. Cir. 2007) ("[A]n applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope"); *Seachange Int'l, Inc. v. C-COR Inc.*, 413 F.3d 1361, 1372-73 (Fed. Cir. 2005) ("Where an applicant argues that a claim possesses a feature that the prior art does not possess in order to overcome a prior art rejection, the argument may serve to narrow the scope of the otherwise broad claim language.").

V. CONCLUSION

For the reasons stated above, Linear's motion *in limine* should be denied.

Respectfully submitted,

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Public Version Dated: May 8, 2008
863640/30611

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EXHIBIT 1

THIS EXHIBIT HAS BEEN REDACTED IN ITS ENTIRETY

EXHIBIT 2

XW 1190317

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

July 22, 2004

THIS IS TO CERTIFY THAT ANNEXED IS A TRUE COPY FROM THE RECORDS OF THIS OFFICE OF THE FILE WRAPPER AND CONTENTS OF:

APPLICATION NUMBER: *08/036,047*
FILING DATE: *March 23, 1993*
PATENT NUMBER: *5,481,178*
ISSUE DATE: *January 02, 1996*

PART (2) OF (9) PART(S)

By Authority of the
COMMISSIONER OF PATENTS AND TRADEMARKS

P. SWAIN
Certifying Officer

9206 # 670. 117 92102

PATENTS
LT-26

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

15/B

Applicants	:	Milton E. Wilcox and Randy G. Flatness
Serial No.	:	08/036,047
Filed	:	March 23, 1993
For	:	CONTROL CIRCUIT AND METHOD FOR MAINTAINING HIGH EFFICIENCY OVER BROAD CURRENT RANGES IN A SWITCHING REGULATOR CIRCUIT
Group Art Unit	:	2102
Examiner	:	Shawn Riley

Bowlyng 7/27/95 7-30-95 HP

June 5, 1995

Hon. Assistant Commissioner
for Patents
Washington, D.C. 20231

PETITION FOR EXTENSION OF TIME
AND RESPONSE TO EXAMINER'S ACTION

Sir:

Petition Under 37 C.F.R. § 1.136(a)
For Extension of Time

Pursuant to 37 C.F.R. § 1.136(a), applicants hereby petition for a three-month extension of the shortened statutory period set forth for response to the Examiner's Action dated December 5, 1994. A check in the amount of eight-hundred seventy dollars ($870.00), in payment of the fee set forth in 37 C.F.R. § 1.17(c), is enclosed herewith.

Response to Examiner's Action

In response to the Examiner's Action, dated December 5, 1994, please amend the above-identified patent application as follows:

In the Claims

Please amend claims 1, 66, 80, 97 and 99 as follows:

1. (Twice amended) A circuit for controlling a switching voltage regulator, the regulator having (1) a switch

B1

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circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output capacitor coupled thereto for supplying current at a regulated voltage to a load, the control circuit comprising:

a first circuit for monitoring a signal from the output terminal to generate a first feedback signal;

a second circuit for generating a first control signal during a first state of circuit operation, the first control signal being responsive to the first feedback signal to vary the duty cycle of the switching transistors to maintain the output terminal at the regulated voltage; and

B1 Concl'd

a third circuit for generating a second control signal during a second state of circuit operation to cause both switching transistors to be simultaneously OFF for a period of time if a sensed condition of the regulator indicates that the current supplied to the load falls below a [compares in a predetermined manner to a current] threshold fraction of maximum rated output current for the regulator, whereby operating efficiency of the regulator at low output current levels is improved.

34~~66~~. (Twice amended) A circuit for controlling a switching voltage regulator, the regulator having (1) a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output capacitor coupled thereto for supplying current at a regulated voltage to a load, the control circuit comprising:

B2

a first means for generating a voltage feedback signal indicative of the voltage at the output;

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a second means for generating a first control signal during a first state of circuit operation, the first control signal being responsive to the voltage feedback signal to vary the duty cycle of the switching transistors to maintain the output terminal at the regulated voltage; and

a third means for generating a second control signal during a second state of circuit operation to cause both switching transistors to be simultaneously OFF for a period of time if a sensed condition of the regulator indicates that the current supplied to the load falls below a threshold fraction of maximum rated output current for the regulator, the period of time having a duration which is a function of the current supplied to the load by the regulator.

B2 Cont'd

41. (Twice amended) A method for controlling a switching voltage regulator, the regulator having (1) a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output capacitor coupled thereto for supplying current at a regulated voltage to a load, the method comprising the steps of:

B3

(a) monitoring a signal from the output terminal to generate a first feedback signal;

(b) varying the duty cycle of the switching transistors in response to the first feedback signal to maintain the output terminal at the regulated voltage during a first state of circuit operation;

(c) turning both switching transistors simultaneously OFF for a period of time during a second state of circuit operation following the first state of circuit operation, so as to allow the output capacitor to maintain the output substantially at the regulated voltage by discharging during

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[a] the second state of circuit operation, the period of time beginning when the current supplied to the load falls below a threshold fraction of maximum rated output current for the regulator, and having a duration which is a function of the current supplied to the load by the regulator; and

(d) turning at least one of said switching transistors ON to recharge the output capacitor following the second state of circuit operation.

B3 Cont'd

55. (Amended) A circuit for controlling a switching voltage regulator, the regulator having (1) a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output capacitor coupled thereto for supplying current at a regulated voltage to a load, the control circuit comprising:

B4

drive circuitry for the pair of synchronously switched switching transistors;

feedback circuitry, coupled to the drive circuitry to control the duty cycle of the pair of synchronously switched switching transistors, the feedback circuitry forming a feedback path in the regulator between the output circuit and the drive circuitry by which feedback information indicative of the current supplied to the load by the regulator conditions the duty cycle of the pair of synchronously switched switching transistors; and

logic circuitry, coupled to the feedback circuitry and the drive circuitry, which prevents the drive circuitry from turning on either of the pair of synchronously switched switching transistors [when] if the feedback information indicates that the current supplied to the load by the

lol

B4

regulator falls below [compares in a predetermined manner to] a selected sleep mode current level[.]. wherein the synchronously switched switching transistors are prevented from being turned on for a period of time that is a function of the current supplied to the load by the regulator.

57. 95. (Amended) An improved circuit for controlling a switching voltage regulator, the regulator having (1) a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors and (2) an output circuit including an output terminal and an output capacitor coupled thereto for supplying current at a regulated voltage to a load, and wherein the control circuit varies the duty cycle of the switching transistors to maintain the output terminal at the regulated voltage, the improvement comprising:

B5

circuitry incorporated in the control circuit for detecting a condition in the output circuit indicative of the current supplied to the load falling below a threshold [value] fraction of maximum rated output current for the regulator and for turning off both switching transistors simultaneously [when] for a period of time if the supplied current falls below the threshold [value], the period of time having a duration which is a function of the current supplied to the load by the regulator.

REMARKS

Summary of Examiner's Action

Claims 1-33, 66-72, 80-82, and 86-99 are pending in this application.

*The Examiner has rejected claims 1-33, 66-72, 80-82, 86-96, and 99 under 35 U.S.C. § 103 as being unpatentable over Inam, et al., U.S. Patent No. 5,177,676 (hereinafter "Inam"),

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in view of Josephson, U.S. Patent 4,706,177 (hereinafter "Josephson").

The Examiner has rejected claims 97 and 98 under 103 U.S.C. § 103 as being unpatentable over Inam and Josephson as applied to claims 1-33, 66-72, 80-82, 86-96, and 99, and further in view of Fung et al., U.S. Patent 5,184,129 (hereinafter "Fung").

Summary of Applicants' Response

Applicants respectfully traverse the Examiner's rejections.

Applicants' invention is directed to maintaining high efficiency in a switching voltage regulator circuit by providing two states of circuit operation. At high load current levels, the circuit provides a regulated DC output voltage by alternatively turning on and off the two transistors of a push-pull switch. When the output current of the regulator drops below a threshold level--i.e. below some fraction (e.g., 20%) of the regulator's maximum rated output current--the regulator's switching transistors are turned off simultaneously for a period of time while previously stored energy in the regulator's output circuit supplies current to the load. This two-state technique for improving efficiency would not have been obvious from an AC power source circuit that disables its output during an overload (the asserted combination of Inam and Josephson), or from an AC power source that goes into a sleep mode when it is not functioning (Inam and Fung).

In accordance with the above, applicants have amended claims 1, 66, 80, 97 and 99 to more particularly point out and distinctly claim that the switching transistors of applicants'

regulator are turned off if the current supplied to the load falls below a threshold level.

Applicants' Response to the Rejection of Claims 1-33, 66-72, 80-82, 86-96, and 99

Applicants respectfully traverse the Examiner's rejections of claims 1-33, 66-72, 80-82, 86-96, and 99 based on Inam and Josephson.

The Examiner acknowledges that "Inam et al. do not show a circuit simultaneously turning off both switching transistors in response to a predetermined threshold." However, the Examiner characterizes Figure 1 of Josephson as showing a circuit which synchronously shuts off transistors 16 and 18 in response to a predetermined threshold. The Examiner asserts that it would have been obvious to include such a circuit into the circuit of Inam "for the purpose of disabling the output as a function of the amplitude and time duration of the overcurrent condition." Applicants' respectfully submit that the inclusion of Josephson's circuit into Inam's circuit, as the Examiner suggests, would not result in applicants' claimed invention.

Both Inam and Josephson are directed to circuits that supply AC power. These circuits cannot be operated in a state in which the AC output voltage is supplied to a load while all switching transistors are turned off. Simultaneously turning off the switching transistors in such circuits for efficiency at low load currents would disrupt the output AC waveform. This is confirmed by Josephson, which as noted by the Examiner states that turning off the transistors disables the output.

Accordingly, while Josephson teaches turning off transistors during overcurrent conditions, a form of current limiting, to purposely prevent the coupling of power to the load, modification of Inam's AC source to incorporate this

teaching would only provide Inam with overload protection, and not a state of regulator operation that improves efficiency at low output current levels. Moreover, there can be no suggestion in these references to improve efficiency by turning off the switching transistors at low output currents because the AC regulation would then be rendered inoperable.

Applicants' amendments to claims 1, 66, 80, 97 and 99 more particularly point out and distinctly claim that the switching transistors of the regulator turn off simultaneously under low output current, rather than overcurrent, conditions. As recited in claims 1, 66, 80 and 99, the threshold output current dividing the two states of operation of the regulator is a fraction of the regulator's maximum rated output current (see, e.g., the specification at pages 12-16).

Claims 86 and 93 are directed to a different feature of the present invention and recite that the output circuit is de-coupled from ground under polarity reversal (low load) conditions. Josephson is even less pertinent to these claims, as Josephson is directed towards de-coupling the output from the power source (not ground), in order to limit current.

In short, Josephson and Inam do not make obvious turning off switching transistors specifically under low output current conditions as recited in applicants' claims. Josephson teaches current limiting to turn off switching transistors to protect them from overcurrents (Josephson, column 2, lines 28-34). Conversely, the synchronous switching regulator of the applicants' invention changes operating state under low output current conditions, the precise opposite of the conditions which motivate the desire to turn off the transistors in Josephson's circuit. Furthermore, applicants' invention is directed towards saving power, a benefit neither Josephson nor Inam teaches or suggests.

For at least the above reasons, improving the efficiency of synchronously switched regulators at low output currents, which is the problem solved by applicants, is unrelated to Josephson's overcurrent protection problem, and it would not have been obvious to look to Inam and Josephson, alone or in combination, for a technique of increasing switching regulator efficiency at low output currents.

Applicants' Response to the
Rejection of Claims 97 and 98

Applicants respectfully traverse the Examiner's rejections of claims 97 and 98 under 35 U.S.C. § 103 as being unpatentable over Inam and Josephson in view of Fung.

The Examiner asserts that it would have been obvious to use the sleep mode circuit as taught by Fung in combination with Inam's voltage source, because Fung (as interpreted by the Examiner) states "that such a modification would reduce current surges thereby minimizing power utilization when main circuit utilizing transistors is not functioning." Here, again, applicants' claimed invention involves conserving power while the regulator is functioning. Moreover, the current surges mentioned in the cited portion of Fung are those occurring as a result of switching between normal operating mode and sleep mode. They are unrelated to load current.

Fung discloses sleep mode circuitry that disables a digital-to-analog converter (DAC) "so as to minimize power utilization when the DACs are not used " (Fung, column 1,lines 39-40). In contrast, applicants use sleep mode to refer to a mode of operation of a voltage regulator that continues to function by supplying current at a regulated voltage. Unlike applicants' claimed circuit, Fung's DAC could not continue to provide the desired output when the circuit is maintained off in sleep mode. Thus, Fung would have provided no motivation to

increase operating efficiency of a circuit by placing it in sleep mode.

Conclusion

Applicants respectfully submit that this application is in condition for allowance. Entry of this amendment, and reconsideration and prompt allowance of this application, including claims 1-33, 66-72, 80-82, and 86-99, are respectfully requested.

Respectfully submitted,

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I Hereby Certify that this Correspondence is being Deposited with the U.S. Postal Service as First Class Mail in an Envelope Addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on June 5, 1995

Dalene Qulachon-Rosen
Name of Person Signing

Dalene Qulachon-Rosen
Signature of Person Signing

EXHIBIT 3

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/036,047	03/23/93	WILCOX	LT-26

RILEY, S EXAMINER

21M1/0807

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ART UNIT	PAPER NUMBER
2111	16

DATE MAILED: 08/07/95

NOTICE OF ALLOWABILITY

PART I.

1. ☑ This communication is responsive to 9 June 1995
2. ☑ All the claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice Of Allowance And Issue Fee Due or other appropriate communication will be sent in due course.
3. ☑ The allowed claims are 1-33, 66-72, 80-82, 86-99
4. ☑ The drawings filed on 29 July 94 are acceptable.
5. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has [...] been received. [...] not been received. [...] been filed in parent application Serial No. _____, filed on _____.
6. ☐ Note the attached Examiner's Amendment.
7. ☐ Note the attached Examiner Interview Summary Record, PTOL-413.
8. ☐ Note the attached Examiner's Statement of Reasons for Allowance.
9. ☐ Note the attached NOTICE OF REFERENCES CITED, PTO-892.
10. ☑ Note the attached INFORMATION DISCLOSURE CITATION, PTO-1449.

PART II.

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" indicated on this form. Failure to timely comply will result in the ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

1. ☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
2. ☐ APPLICANT MUST MAKE THE DRAWING CHANGES INDICATED BELOW IN THE MANNER SET FORTH ON THE REVERSE SIDE OF THIS PAPER.
   a. ☐ Drawing informalities are indicated on the NOTICE RE PATENT DRAWINGS, PTO-948, attached hereto or to Paper No. _____. CORRECTION IS REQUIRED.
   b. ☐ The proposed drawing correction filed on _____ has been approved by the examiner. CORRECTION IS REQUIRED.
   c. ☐ Approved drawing corrections are described by the examiner in the attached EXAMINER'S AMENDMENT. CORRECTION IS REQUIRED.
   d. ☐ Formal drawings are now REQUIRED.

Any response to this letter should include in the upper right hand corner, the following information from the NOTICE OF ALLOWANCE AND ISSUE FEE DUE: ISSUE BATCH NUMBER, DATE OF THE NOTICE OF ALLOWANCE, AND SERIAL NUMBER.

Attachments:

- Examiner's Amendment
- Examiner Interview Summary Record, PTOL-413
- Reasons for Allowance
- Notice of References Cited, PTO-892
- Information Disclosure Citation, PTO-1449
- Notice of Informal Application, PTO-152
- Notice re Patent Drawings, PTO-948
- Listing of Bonded Draftsmen
- Other

PETER S. WONG
SUPERVISORY PATENT EXAMINER
GROUP 2100

PTOL-37 (REV. 4-89) *

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

CERTIFICATE OF SERVICE

I, David E. Moore, hereby certify that on May 8, 2008, the attached document was electronically filed with the Clerk of the Court using CM/ECF which will send notification to the registered attorney(s) of record that the document has been filed and is available for viewing and downloading.

I further certify that on May 8, 2008, the attached document was Electronically Mailed to the following person(s):

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